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Question Paper Code : 51405

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2014.

Fifth Semester

Electronics and Communication Engineering

EC 2303/EC 53/10144 EC 605 — COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Sixth Semester Biomedical Engineering)

(Regulation 2008/2010)

(Common to PTEC 2303 – Computer Architecture and Organization for B.E. (Part-Time) Fourth Semester, Electronics and Communication Engineering, Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Let $x = 1010100$ and $Y = 1000011$. Perform

   (a) X-Y and

   (b) Y-X using 1's complement.

2. What is a co-processor?

3. What is a full adder and how many full adders are required to construct a 4-bit full adder?

4. Draw a space-time diagram for a six-segment pipeline showing the time it takes to process six tasks.

5. What is an instruction pipeline?

6. Differentiate between hardwired and micro programmed control.

7. What is a cache memory?

8. Differentiate between static and dynamic RAM.

9. What is meant by handshaking signals?

10. What is meant by bus arbitration?

PART B — (5 × 16 = 80 marks)

11. (a) (i) What are integrated circuits? Describe the evolution of IC's in detail. (8)

(ii) What is a priority encoder? Design a 16-bit priority encoder using two copies of an 8-bit encoder. (8)

Or

(b) (i) What is a multiplexer? Construct an eight-input multiplexer using two-input multiplexers. (8)

(ii) Discuss about the general approach to the design of register-level systems. (8)

12. (a) (i) Illustrate the Robertson multiplication algorithm for two's-complement fractions with an example. (8)

(ii) Draw the block diagram of a four-stage floating-point adder pipeline and illustrate the behavior. (8)

Or

(b) (i) Give the non-restoring division algorithm for unsigned integers and illustrate with an example. (8)

(ii) Design a 8-bit adder-subtracter using 4-bit adders and explain the behavior of the circuit. (8)

13. (a) Discuss about the design of hardwired control unit for a two's-complement multiplier. (16)

Or

(b) Explain various factors that reduce the performance of the pipeline and how they can be overcome.

14. (a) (i) What is associate memory? Draw the block diagram of associate memory and explain how the read and write operations performed in associate memory. (10)

(ii) What are the advantages and disadvantages of pre-emptive and non-preemptive memory allocation? (6)

Or

(b) (i) What are the major differences between the following memory technologies : SRAMs, flash memories, magnetic floppy disks, optical disks and CD ROMs? (8)

(ii) Consider a typical RAM chip of 128×2. Explain how to construct a memory system of 512×2 and 128×8 using suitable number of RAM chips. (8)

15. (a) (i) Explain how fault tolerance is achieved using hardware and software redundancy. (10)

(ii) What is vector processing? Draw the architecture of a typical vector processor and explain. (6)

Or

(b) (i) With the help of a block diagram, explain the daisy-chaining method of establishing priority among the interrupting devices. (8)

(ii) What is IOP? Explain how CPU and IOP communicate with each other. (8)
